Listing of the Claims:

The following is a complete listing of all the claims in the application, with an indication of the status of each:

1 (Original). A field effect transistor comprising:

a) a channel doping region;

b) a gate insulator disposed above the channel doping region;

c) a gate electrode disposed above the gate insulator; and

d) at least one underlap region adjacent to the channel doping region positioned between either a source extension or a drain extension and said channel doping region which does not underlap the boundaries of the gate electrode, wherein either

a resistance of said underlap region is no more than 30% of an ON-state resistance of said channel doping region, or

the underlap region has a doping level no more than 1 x 10^{17}/cc over a lateral thickness equal to or greater than a thickness of the gate insulator.

2. (Original) The field effect transistor of claim 1, further comprising a source extension and a drain extension, and wherein said at least one underlap region includes a first underlap region positioned between said source extension and said channel doping region and a second underlap region positioned between said drain extension and said channel doping region.

3. (Original) The field effect transistor of claim 1 wherein the at least one underlap region has a doping level less than 5 x 10^{16}/cc over a lateral thickness equal to or greater than a thickness of the gate insulator.

4. (Original) The field effect transistor of claim 1 wherein the at least one underlap region has a doping level less than 1 x 10^{15}/cc over a lateral thickness equal to or greater than a thickness of the gate insulator.

5. (Original) The field effect transistor of claim 1 wherein the at least one underlap region has a doping level less than 5 x 10^{16}/cc over a lateral thickness equal to or

greater than twice a thickness of the gate insulator.

6. (Original) The field effect transistor of claim 1 wherein the at least one underlap region has a doping level less than 1 x 10^{15}/cc over a lateral thickness equal to or greater than twice a thickness of the gate insulator.

7. (Original) The field effect transistor of claim 1 wherein the at least one underlap region has a lateral thickness in the range of 3-15 nanometers.

8. (Original) The field effect transistor of claim 1 wherein the at least one underlap region has a resistance of less than about 20 % of an ON-state resistance of the channel doping region.

9. (Original) The field effect transistor of claim 1 wherein the at least one underlap region has a resistance of less than about 15 % of an ON-state resistance of the channel doping region.

10. (Original) The field effect transistor of claim 1 wherein the at least one underlap region has the same conductivity type as the channel doping region.

11. (Original) The field effect transistor of claim 1 wherein the at least one underlap region has the opposite conductivity type as the channel doping region.

12. (Original) The field effect transistor of claim 1 wherein the field effect transistor is a finFET.

13. (Original) The field effect transistor of claim 1 wherein the channel doping region is narrower than the gate.

14. (Currently amended) An electronic circuit, comprising:

a) at least one field effect transistor comprising:

a channel doping region;

a gate insulator disposed above the channel doping region;

a gate electrode disposed above the gate insulator;

at least one underlap region adjacent to the channel doping region positioned between either a source extension or a drain extension and said channel doping region which does not underlap the boundaries of the gate electrode, wherein either

a resistance of said underlap region is no more than 30% of an ON-state resistance of said channel doping region, or

the underlap region has a doping level no more than 1×10^{17}/cc over a lateral thickness equal to or greater than a thickness of the gate insulator;and :

b) a voltage supply operable for providing voltage to the field effect transistor so that the field effect transistor is operated with a gate voltage of less than about 130% of a threshold voltage.

15. (Original) The electronic circuit of claim 14 wherein the voltage supply is operable for providing voltage to the field effect transistor so that the field effect transistor is operated with a gate voltage of less than about 100% of the threshold voltage.

16. (Original) The electronic circuit of claim 14 wherein the voltage supply is operable for providing voltage to the field effect transistor so that the field effect transistor is operated with a gate voltage of less than about 80% of the threshold voltage.

17. (Original) The electronic circuit of claim 14 wherein said at least one field effect transducer comprises a plurality of field effect transducers wherein each of the plurality of field effect transducers have the same threshold voltage to within about 10%.

18 (Currently amended). The electronic circuit of claim 14 ~~23~~ wherein the field effect transistor has two underlap regions, with one underlap region on each side of the channel doping region.